IN THE SPECIFICATION

Please amend paragraph 4 as follows:

[0004] While this conventional solution may provide additional interface capabilities between an IC and circuit components, it has a number of limitations. For one, the addition of the control register 120 increases the complexity of the system. Likewise, the addition of the control register 120 typically increases the cost of development and manufacture of a system utilizing such a solution, as well as increases the size and power consumption of such a[[s]] system.

Please amend paragraph 22 as follows:

[0022] As illustrated in Figure 2, the five circuit components 111-115 desired to interface with the IC 110 exceed[[s]] in number the four available GPIO lines 101-104. Known solutions, as discussed previously, typically require additional hardware to connect additional circuit components to the IC 110. However, in the event that there is at least one circuit component of circuit components 111-115 that only provides an input to the IC 110 and at least one circuit component that only receives an output from the IC 110, then these at least two of circuit components 111-115 (one to provide an input and one to receive an output) can share a single GPIO line 101-104 provided that either their input and output occur at essentially separate times or that their operation is not significantly effected by the switching of the GPIO line between an input line and an output line.

Please amend paragraph 25 as follows:

[0025] In at least one embodiment, output to circuit component 115 and input from circuit component 114 may be attempted concurrently due to a high switching frequency of the shared GPIO line between an input line to an output line. For example, circuit component 114 can include a switch and circuit component 115 can include a LED. In this example, the IC 110 can switch between an input line to receive input caused by activating the switch (circuit component 114) and an output line to provide a voltage to the LED (circuit component 115). If the GPIO line 104 acts as an output line more often than an input line, thenthan the appearance of the LED typically is unaffected, assuming the GPIO line 104 is switched faster than the

human flicker-fusion rate. Likewise, because the typical human reaction time is about 0.20 seconds and because the period between two input states of the GPIO line 104 typically is much less than this reaction time, the GPIO line 104 is switched to an input line during the switch activation period, and therefore the input from the switch is noted by the IC 110.

Please amend paragraph 29 as follows:

[0029] As illustrated in Figure 4, the IC 110 can configure the GPIO direction register 240 to set the I/O direction assembly 204 to allow data or a signal to be output on the GPIO line 104 during a second time period (t=2). The IC 110 can then write data to the output buffer 214 during this second time period, where it is then provided to the circuit component 115 via the GPIO line 104. In this manner, the IC 110 may alternate between receiving from and providing data to~~from~~ circuit components 114, 115, respectively, as desired.

IN THE CLAIMS

Please amend claims 1, 8 and 28 as follows:

Claim Listing:

1. (CURRENTLY AMENDED) A method for sharing a ~~single~~ general purpose input/output (GPIO) line of an integrated circuit between at least two circuit components, the method comprising:

providing, using the GPIO line, a first input from a first circuit component to the integrated circuit during a first time;

providing, using the GPIO line, a first output from the integrated circuit to a second circuit component during a second time; and

wherein the first circuit component and the second circuit component are concurrently coupled to the GPIO line.

2. (ORIGINAL) The method of Claim 1, wherein the step of providing the first input includes providing the first input at a low frequency relative to a switching frequency of the GPIO line.

3. (ORIGINAL) The method of Claim 2, wherein the first time is at least in part concurrent with the second time.

4. (ORIGINAL) The method of Claim 1, wherein the first time is different from the second time.

5. (ORIGINAL) The method of Claim 1, further comprising the step of providing, using the GPIO line, a second input from the first circuit component to the integrated circuit during a third time different from the first time.

6. (ORIGINAL) The method of Claim 1, further comprising the step of providing, using the GPIO line, a second output from the integrated circuit to the second circuit component during a third time different from the second time.

7. (ORIGINAL) The method of Claim 1, wherein the step of providing a first input comprises the step of configuring the GPIO line as an input line during a portion of the first time, and the step of providing a first output comprises the step of configuring the GPIO line as an output line during the second time.

8. (CURRENTLY AMENDED) The method of Claim 7, wherein:
the portion of the first time includes a first sequence of processing cycles; and
the second time includes a second sequence of processing cycles different from the first sequence.

9. (ORIGINAL) The method of Claim 1, wherein the first circuit component includes a switch.

10. (ORIGINAL) The method of Claim 1, wherein the second circuit component includes a light emitting diode.

11. (ORIGINAL) The method of Claim 10, wherein the second circuit component further includes an inverter.

12. (ORIGINAL) The method of Claim 1, wherein the integrated circuit comprises one or more of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.

13. (ORIGINAL) A method for sharing a general purpose input/output (GPIO) line of an integrated circuit, the method comprising:
connecting a first circuit component to the GPIO line;
connecting a second circuit component to the GPIO line concurrently with the first circuit component;
wherein the first circuit component is to provide input to the integrated circuit using the GPIO line during a first time; and

wherein the second circuit component is to receive an output from the integrated circuit using the GPIO line during a second time.

14. (ORIGINAL) The method of Claim 13, wherein the step of providing the first input includes providing the first input at a low frequency relative to a switching frequency of the GPIO line.

15. (ORIGINAL) The method of Claim 14, wherein the first time is at least in part concurrent with the second time.

16. (ORIGINAL) The method of Claim 13, wherein the first time is different from the second time.

17. (ORIGINAL) The method of Claim 13, further comprising the steps of:
configuring the GPIO line as an input line during a portion of the first time; and
configuring the GPIO line as an output line during the second time period.

18. (ORIGINAL) The method of Claim 17, wherein:
the portion includes a first sequence of processing cycles; and
the second time includes a second sequence of processing cycles different from the first sequence.

19. (ORIGINAL) The method of Claim 13, wherein the first circuit component includes a switch.

20. (ORIGINAL) The method of Claim 13, wherein the second circuit component includes a light emitting diode.

21. (ORIGINAL) The method of Claim 20, wherein the second circuit component further includes an inverter.

22. (ORIGINAL) The method of Claim 13, wherein the integrated circuit is one of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.

23. (ORIGINAL) An electrical circuit having circuit components in electrical communication with an integrated circuit, the circuit being adapted to share a general purpose input/output (GPIO) line of the integrated circuit among at least two circuit components external to the integrated circuit, the circuit comprising:
a first circuit component connected to the GPIO line;
a second circuit component connected to the GPIO line concurrently with the first circuit component;
the integrated circuit being adapted to receive an input from the first circuit component via the GPIO line during a first time; and
the integrated circuit being adapted to provide an output to the second circuit component via the GPIO line during a second time.

24. (ORIGINAL) The circuit of Claim 23, wherein the first circuit is adapted to provide the first input at a low frequency relative to a switching frequency of the GPIO line.

25. (ORIGINAL) The circuit of Claim 24, wherein the first time is at least in part concurrent with the second time.

26. (ORIGINAL) The circuit of Claim 23, wherein the first time is different from the second time.

27. (ORIGINAL) The circuit of Claim 23, wherein the GPIO line is configured as an input line during a portion of the first time, and the GPIO line is configured as an output line during the second time.

28. (CURRENTLY AMENDED) The circuit of Claim 27, wherein the portion of the first time includes a first sequence of processing cycles, and the second time includes a second sequence of processing cycles different from the first sequence.

29. (ORIGINAL) The circuit of Claim 23, wherein the first circuit component includes a switch.

30. (ORIGINAL) The circuit of Claim 23, wherein the second circuit component includes a light emitting diode.

31. (ORIGINAL) The circuit of Claim 30, wherein the second circuit component further includes an inverter.

32. (ORIGINAL) The circuit of Claim 23, wherein the integrated circuit comprises at least one of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.

33. (ORIGINAL) In a system comprising electrical circuitry and components:
an integrated circuit having a general purpose input/output (GPIO) line;
a first circuit component coupled to the GPIO line, wherein the first circuit component is adapted to provide, at a first time, a first input to the integrated circuit using the GPIO line; and
a second circuit component coupled to the GPIO line, wherein the second circuit component is adapted to receive, at a second time, a first output from the integrated circuit using the GPIO line.

34. (ORIGINAL) The system of Claim 33, wherein the first circuit component further is adapted to provide the first input at a low frequency relative to a switching frequency of the GPIO line.

35. (ORIGINAL) The system of Claim 34, wherein the first time is concurrent with the second time.

36. (ORIGINAL) The system of Claim 33, wherein the first time is different from the second time.

37. (ORIGINAL) The system of Claim 36, wherein:
the first time includes a first sequence of processing cycles; and
the second time includes a second sequence of processing cycles different from the first sequence.

38. (ORIGINAL) The system of Claim 33, wherein the integrated circuit comprises at least one of a group consisting of: a microprocessor, a microcontroller, a field programmable gate array, a programmable logic device, a programmable logic array, and an application specific integrated circuit.

39. (ORIGINAL) The system of Claim 33, wherein the first circuit component includes a switch.

40. (ORIGINAL) The system of Claim 33, wherein the second circuit component includes a light emitting diode.

41. (ORIGINAL) The system of Claim 40, wherein the second circuit component further includes an inverter.

42. (ORIGINAL) The system of Claim 33, wherein the system comprises a communications modem.

43. (ORIGINAL) The system of Claim 42, wherein the communications modem includes the first and second circuit components.

44. (ORIGINAL) The system of Claim 43, wherein the system is a DSL communications system.

REMARKS

Introduction

The Office Action dated September 9, 2003, has been received and carefully considered. Claims 1-44 are pending in the present application. Claims 1-44 stand rejected. In this response, the specification and claims 1, 8 and 28 have been amended. The amendments to the specification and the claims were made solely to improve their form, readability and/or clarity and were not made to distinguish the claimed subject matter over the cited references. Support for the amendments to the specification and the claims can be found in the original claims, drawings and specification. No new matter is presented by the amendments to the specification and the claims. Accordingly, Applicants respectfully request entry thereof and reconsideration of the pending claims in view of the following remarks.

Anticipation Rejection of Claims 1, 4-8, 12, 13, 16-18, 22, 23, 26-28, 32, 33, 36-38, 42 and 43

At page 2 of the Office Action, claims 1, 4-8, 12, 13, 16-18, 22, 23, 26-28, 32, 33, 36-38, 42 and 43 were rejected under 35 U.S.C. § 102(b) as being anticipated by Marisetty et al. (U.S. Patent No. 5,792,598). This rejection is hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id.

With regard to independent claims 1, 13, 23 and 33, the Examiner asserts that Marisetty discloses a method, apparatus and system comprising: connecting a first circuit component to a

GPIO line; connecting a second circuit component to the GPIO line concurrently with the first component; wherein the first circuit component is to provide input the integrated circuit using the GPIO line during a first time; and wherein the second circuit component is to receive an output from the integrated circuit using the GPIO line during a second time. (Office Action, pp. 2-3). In support of this assertion, the Examiner cites column 5, lines 48-54 and figure elements 104A, 104B and 112 of Marisetty.

In establishing the alleged relevancy of Marisetty to the present invention, the Examiner refers to element 112 of Marisetty as "GPIO line 112" at page 2 of the Office Action. Applicants respectfully submit that the Examiner's description of element 112 as a GPIO line is inconsistent with both the disclosure of Marisetty and the knowledge of one of ordinary skill in the art. Marisetty refers to element 112 as "bus" 112 (e.g., "I/O devices 104A-104C are coupled to shared logic block 103A in PGA 103 via shared bus 112", Marissetty, col. 4, lines 38-39). In discussing bus 112, Marisetty discloses that: "I/O devices 104A-C share *a set of external bus lines 112*. These external *bus lines* may include address, data and control lines." (Marisetty, col. 5, lines 37-39)(emphasis added). Marisetty's description of the bus 112 as a plurality of lines for both addressing and data transmission is consistent with the conventional use of the term "bus." To illustrate, the online encyclopedia Webopedia defines a bus as "[a] *collection of wires* through which data is transmitted from one part of a computer to another. ... *All buses consist of two parts -- an address bus and a data bus*. The data bus transfers actual data whereas the address bus transfers information about where the data should go." (http://www.webopedia.com/TERM/b/bus.html)(emphasis added). Similarly, the online dictionary TechDictionary.com defines a bus as "[a] *set of conductors* which connect the functional units in a computer..." (http://www.techdictionary.com/)(emphasis added).

Thus, a bus, in conventional use and as described by Marisetty, includes a plurality of lines used to connect I/O devices, where the bus includes both address lines for addressing and data lines for communicating data. In contrast, a GPIO line includes a single line used by an integrated circuit (IC) to either input or output a signal. Thus, while the addressing capability provided by the address lines of a bus allow multiple I/O devices to share the data lines of the bus, it will be appreciated that a GPIO line, being a single line, lacks means for addressing,

thereby conventionally preventing the operation of more than one I/O devices on the GPIO line. The present invention, as claimed, addresses and solves this limitation.

As noted above, the shared bus 112 disclosed by Marisetty is not a GPIO line. Further, Marisetty does not teach, disclose, or motivate the sharing of a GPIO line by two or more I/O devices nor does Marisetty disclose any use of a GPIO line. Accordingly, because Marisetty fails to teach, disclose, or suggest, alone or in combination with the remaining cited references, each and every limitation of independent claims 1, 13, 23 and 33, Applicants respectfully submit that Marisetty fails to anticipate independent claims 1, 13, 23 and 33.

Claims 2-12 are dependent upon independent claim 1, claims 14-22 are dependent on independent claim 13, claims 24-32 are dependent on independent claim 23 and claims 34-44 are dependent on independent claim 33. Thus, since independent claims 1, 13, 23 and 33 should be allowable as discussed above, claims 2-12, 14-22, 24-32 and 34-44 should also be allowable at least by virtue of their dependency on one of independent claims 1, 13, 23 or 33.

In view of the foregoing, Applicants respectfully submit that the aforementioned anticipation rejection of claims 1, 4-8, 12, 13, 16-18, 22, 23, 26-28, 32, 33, 36-38, 42 and 43 is obviated, and respectfully request the withdrawal of such rejection.

Obviousness Rejection of Claims 9-11, 19-21, 29-31 and 39-41

At page 4 of the Office Action, claims 9-11, 19-21, 29-31 and 39-41 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Marisetty et al. in view of Applicants' admitted prior art (AAPA). This rejection is hereby respectfully traversed.

The Examiner asserts that although not disclosed by Marisetty, the use of switches, light emitting diodes (LEDs) and inverters on GPIO lines is well known because the use of such is allegedly described in the Background section of the present application. The Examiner therefore concludes that it would have been obvious to one of ordinary skill in the art to modify the teachings of Marisetty to arrive at the invention as claimed by claims 9-11, 19-21, 29-31 and 39-41. This rejection is hereby respectfully traversed.

As noted above, the prior art references cited by the Examiner fail to disclose, teach or suggest, alone or in combination, all of the claimed limitations of independent claims 1, 13, 23,

and 33 from which claims 9-11, 19-21, 29-31 and 39-41 respectively depend. Accordingly, dependent claims 9-11, 19-21, 29-31 and 39-41 should be allowable at least by virtue of their dependency on one of independent claims 1, 13, 23 or 33.

In view of the foregoing, Applicants respectfully submit that the aforementioned obviousness rejection of claims 9-11, 19-21, 29-31 and 39-41 is obviated, and respectfully request the withdrawal of such rejection.

Obviousness Rejection of Claims 2, 3, 14, 15, 24, 25, 34, 35 and 44

At page 5 of the Office Action, claims 2, 3, 14, 15, 24, 25, 34, 35 and 44 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Marisetty et al. in view of Amrany et al. (U.S.Patent No. 6,580,752). This rejection is hereby respectfully traversed.

The American Inventors Protection Act of 1999 amended 35 U.S.C. § 103(c) to prevent subject matter that qualifies as prior art under 35 U.S.C. § 102(e) from precluding patentability where the subject matter and the claimed invention were, at the time the invention was made, owned by the same entity or subject to an obligation of assignment to the same entity. Applicants hereby declare that the claimed invention and the invention of Amrany were owned by the same entity and subject to an obligation of assignment to the same entity, namely GlobespanVirata, Inc. of Redbank, New Jersey, at the times the respective inventions were made. Accordingly, Applicants respectfully submit that Amrany does not qualify as applicable prior art under 35 U.S.C. § 102(e) in view of 35 U.S.C. § 103(c) as amended.

Further, as noted above, the prior art references cited by the Examiner fail to disclose, teach or suggest, alone or in combination, all of the claimed limitations of independent claims 1, 13, 23, and 33 from which claims 2, 3, 14, 15, 24, 25, 34, 35 and 44 respectively depend. Accordingly, dependent claims 2, 3, 14, 15, 24, 25, 34, 35 and 44 should be allowable at least by virtue of their dependency on one of independent claims 1, 13, 23 or 33.

In view of the foregoing, Applicants respectfully submit that the aforementioned obviousness rejection of claims 2, 3, 14, 15, 24, 25, 34, 35 and 44 is obviated, and respectfully request the withdrawal of such rejection.

Conclusion

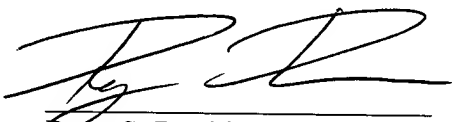
In view of the foregoing, Applicants respectfully submit that the present application is in condition for allowance and earnestly solicit notice to that effect. The Examiner is invited to contact the undersigned at the below listed telephone number to expedite resolution of any issues or to address any comments, questions, or suggestions that may arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,

HUNTON & WILLIAMS LLP

Date: October 7, 2003

By: 

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